REMARKS

Applicant has considered the Office Action dated July 24, 2007, and the references cited therein. Claims 1-13, 15, and 16 are currently pending. No claims presently stand allowed. Applicant has amended the claims to recite that the snapshot buffer includes state information provided from the internal processor pipeline. The modifications to the controller means are primarily to reverse previously submitted amendments. The "state information from the internal processor pipeline" language added to claim 1 is supported by at least the portion of the original specification corresponding to paragraph [0003] of Leijten US Pub. No. 2005/0262389.

In summary of the remarks below, Applicant traverses the rejections of each and every one of the claims under 35 U.S.C. §§ 102, 103, and/or 112. All amendments to the original claims are fully supported by the original disclosure of the present application.

Regarding the rejections based upon prior art, the Cohen patent, upon which the rejection of the present pending claims relies, neither discloses nor suggests at least one recited element within each of the presently pending claims. For example, the invention as recited in claim 1 is directed to a data processor that embodies a new way of handling multiple and nested interrupts using a secondary data storage level. The data processor includes a snapshot buffer for saving a snapshot of processor state information, *including state information from an internal processor pipeline*, during the handling of an interrupt condition, and controller means which saves the contents of the snapshot buffer in a data memory facility having a multibit access port facility upon occurrence of a "nested" interrupt condition. Applicant directs specific attention to the portion of amended claim 1 that recites the state information includes *state information from the internal processor pipeline* – supported, for example at paragraph [0003] of Applicant's published application. Thus, in accordance with the invention recited in claim 1, a snapshot is made of the internal processor pipeline state at the time of each interrupt (whether first level or nested). After completing an interrupt, the data processor restores the previous pipeline state from the snapshot buffer. In the case of a nested interrupt, the claimed control means transfers the contents of the snapshot buffer to the data memory (including a multibit access port). Cohen neither discloses nor suggests the above-recited elements of the claimed data processor.

In contrast to the claimed invention, the Cohen reference discloses a microprocessor including three classes of registers: those which are always duplicated and stacked automatically (the unprimed and prime registers); those which are duplicated, but only stacked as necessary and under software control; and those which are not duplicated and are stacked only if necessary and under software control (the other registers.) (*see, e.g.*, Cohen, col. 5, lines 8-15). Thus, only the content of the prime and unprimed registers is duplicated and saved on stack automatically. The unprimed and prime registers comprise a status register SR, a context switch control register, and a program counter PC. (Cohen, col. 3, lines 29-45). Cohen does not disclose or suggest storing the results of the *internal processor pipeline*, as presently recited in the claims.

Applicant therefore requests favorable reconsideration of the Final Office Action's grounds for rejecting the previously pending claims in view of Applicant's amendments to the previously pending claims and the Remarks provided herein below. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of the Rejections

1. Claims 1-13, 15, and 16 are rejected under 35 U.S.C. §112, second paragraph, as failing to comply with the written description requirement.

2. Claims 1-3, 5-7, 9, and 13 are rejected as being anticipated under 35 U.S.C. §102(b) in view of U.S. Patent No. 5,115,506 to Cohen et al. (Cohen).

3. Claim 4 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of U.S. Patent No. 5,958,041 to Petolino, Jr. et al. (Petolino).

4. Claim 8 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Paterson et al. (*Computer Organization & Design: The Hardware/Software Interface*).

5. Claims 15 and 16 are rejected under 35 U.S.C. §103(a) as being obvious over Cohen.

6. Claim 10 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of U.S. Patent No. 5,448,705 to Nguyen et al. (Nguyen).

7. Claim 11 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Lang et al. (*Individual Flip-Flops with Gated Clocks for Low Power Datapaths*).

8. Claim 12 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Shen et al. (*Modern Processor Design: Fundamentals of Superscalar Processors*).

Applicant traverses the grounds for each and every rejection for at least the reasons set forth herein below. Applicant addresses the specific rejections in the order they arise in the Final Office Action.

Applicant Traverses the § 112 Rejection of Claims 1-13, 15, and 16 as Failing to Comply with the Written Description Requirement

The Final Office Action requests Applicant to provide evidence that all newly claimed subject matter in claims 1, 9, 15 and 16 is supported by the original disclosure of the application. Applicant address the substantive amendments, occurring both in this Amendment and the Amendment filed in response to the non-final Office Action of 12 April 2007, of the claims in numerical order. All references are to paragraphs within Applicant's US Pub. No. 2005/0262389.

Claim 1 was *previously* amended to clarify that the controller means is arranged to save the contents of the snapshot buffer elements "upon a subsequent interrupt condition that occurs during the handling of an actual interrupt condition without requiring instruction bits for addressing the snapshot buffer elements or the data memory facility additional to information of the stack pointer of the snapshot buffer." With regard to this language (now present in new dependent claim 17), the specification, at paragraph 19, explains that, in an embodiment, because "the snapshot buffer will maintain its own internal stack pointer, none of the above read/write commands will require a register address, as would have been required for standard random access register files." As a result, the paragraph explains, "no additional instruction bits will be required for addressing the registers in the snapshot buffer." Therefore, this previously submitted claim language previously added to claim 1 in a

previous amendment, and now deleted from claim 1 and re-submitted in claim 17, is supported by the specification.

Claim 1 is *currently* amended to recite that the information of various processor state elements includes "state information from the internal processor pipeline." With regard to the support for this amendment, Applicant notes that paragraph [0024] describes that the invention is advantageous to various interruptible embedded processor architectures that employ scheduling based on Non Unit Assumed Latency with Equal semantics (NUAL-EQ) that require pipeline snapshots instead of pipeline flushing. NUAL-EQ semantics are described in detail in paragraphs [0002] and [0003]. Paragraph [0003] specifically notes that NUAL-EQ semantics require that an exact snapshot be taken from the internal processor pipeline. Therefore, this current amendment of claim 1 is supported by the original specification.

Claim 9 was amended to include the limitation "wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility, wherein said snapshot buffer comprises output multiplexor means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility." In addition, claim 9 was amended to clarify that the write and read operations in the stack are executed at mutually exclusive instants in time "under control of a stack pointer." Applicant respectfully points out that the snapshot buffer with the claimed limitations is described fully and in substantial detail in paragraphs 17-18 and FIG. 2 of the original application. In particular, the specification describes the operation of the input multiplexor (demultiplexor 54), the output multiplexor (multiplexor 56), and how the input multiplexor and output multiplexor are controlled by a stack pointer from a stack register 58. Paragraph 19 describes that the snapshot buffer elements are sequentially saved. Therefore, the amendments to claim 9 are supported by the specification.

Claims 15 and 16 recite that the controller means "saves" and "restores" in a single clock cycle. These claim elements are recited by the disclosure at paragraph [0021] of the published application.

Applicant Traverses the § 102(b) Rejection of Claims 1-3, 5-7, and 9 as Anticipated by Cohen

Applicant traverses the rejection of **claim 1** because Cohen neither discloses nor suggests at least one recited element of Applicant's claimed data processor that incorporates a control means that supports a specific way of handling nested interrupts. In particular, Cohen does not disclose or suggest a snapshot buffer which, during the handling of an interrupt condition, accommodates saving state information of various processor state elements "including state information from the internal processor pipeline." In fact, the only state information that Cohen discloses is state information that is the result of operations carried out by the processor.

In particular, Cohen teaches that the prime 22 and unprime 20 registers are the only registers whose contents are automatically placed on a stack during multiple overlapping (i.e., nested) interrupt conditions. (Cohen, col. 4, lines 25-48). The prime and unprimed registers comprise a status register SR, a context switch control register CSC and a program counter PC (col. 3, lines 29-45). Cohen does not disclose the details of the content of the status register SR, but does make reference to the Motorola 68000 series of microprocessors. As can be seen on page 364 of the product specification for a 68000 processor, attached hereto as Exhibit A, the upper byte of the status register is available to the programmer and, therefore, the result of operations carried out by the processor and not from the internal processor pipeline. Therefore, Applicant respectfully submits that claim 1 is not anticipated by Cohen for at least this reason.

In addition, with regard to the portion of claim 1 now presented as dependent claim 17, Cohen neither discloses nor suggests that the controller means saves snapshot buffer elements in a data memory facility without requiring instruction bits for addressing the snapshot buffer elements or the data memory facility beyond/additional to information of the stack pointer of the snapshot buffer. The Final Office Action argued that "[t]here is no limitation in the claim that requires *no* bits are required, only that no *additional instruction* bits are required." Therefore, Applicant has amended the element previously added to claim 1 (now in claim 17) to clarify that no instruction bits other than those of the stack pointer of the snapshot buffer are required to address the buffered snapshot information. As Applicant has stated previously, the structure disclosed in Cohen requires information bits *additional to*

those of a stack pointer in the snapshot buffer. Therefore, Applicant respectfully submits that independent claim 17 is not anticipated by Cohen for at least this additional reason.

The remaining claims are dependent on claim 1 and, therefore, Applicant respectfully submits that the remaining claims are not anticipated by Cohen for at least the reason that each of the dependent claims (from independent claim 1) includes at least one element that is not disclosed in Cohen.

Applicant Traverses the § 103(a) Rejections of Claims 4, 8, 10-12, 15, and 16 as Obvious Over Cohen in View of Other Prior Art References

As noted above, claim 1, is not anticipated by Cohen at least because Cohen does not disclose or suggest the above-identified claim limitations. The claim limitations identified above are also not disclosed or suggested by the other references cited in the Final Office Action. Therefore, Applicant respectfully submits that claims 4, 8, 10-12, 15, and 16 are not obvious under 35 U.S.C. 103(a).

Applicants specifically address the obviousness rejection of **claim 12**, which is currently further amended to recite that the data processor is a "VLIW (very long instruction word) processor". This amendment is supported by the disclosure at paragraph [0016] of the published application. It is by no means obvious to have several issue slots in a VLIW data processor wherein only a single issue slot is used for implementing handling of nested interrupts. The superscalar processor disclosed in Shen at pages 175 and 177 comprises a single issue slot, wherein instructions are dispatched to reservation stations for various functional units. From the reservation stations the instructions are issued at run-time to the functional units, i.e. a branch unit, an integer unit, a floating-point unit and a load-store unit.

Shen does not disclose or suggest use of only a single issue slot of many issue slots in a data processor to handle saving snapshot data in response to multiple overlapping (nested) interrupts occurring on the data processor. Shen gives no idea how an interrupt should be carried out on the superscalar depicted in FIG. 4-26. Even if an "issue unit" is the same as an "issue slot", it still cannot be envisioned how the processor of FIG. 4-26 (a single issue unit) would not suffice to carry out an interrupt process. Instead, servicing an interrupt would require, in addition to the load/store unit, at least a branch unit. For example, at page 175, Shen states "Typically, even with function units that require multiple-cycle latencies, once an

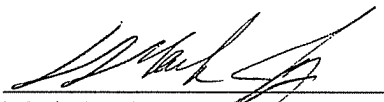
instruction begins execution in a pipelined functional unit, there is no further stalling of that instruction in the middle of the execution pipeline...." This quote also suggests that the processor of FIG. 4-27 is not arranged to handle an interrupt in a single clock cycle (see, claims 15 and 16). Applicant's disclosed/claimed data processor facilitates handling a single interrupt, in a single clock cycle in a pipeline processor arrangement, by storing the status of internal pipeline processor components to the claimed snapshot buffer.

Furthermore, it would not be obvious, to apply the processor architecture of FIG. 4-26 in Shen to a VLIW processor. The processor disclosed in Shen is a single issue slot processor wherein instructions are dispatched to reservation stations for various functional units. From the reservation stations the instruction are issued at runtime to the functional nits. In a VLIW processor, however, the instructions are scheduled at compile-time. The saving of the present state of the internal processor pipeline by the control means enables the processor to be "always interruptible" – even when the data processor is already in an interrupted state or when processing a VLIW instruction.

Conclusion

Applicant respectfully submits that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



Mark Joy, Reg. No. 35,562
LEYDIG, VOIT & MAYER, LTD.
Two Prudential Plaza, Suite 4900
180 North Stetson Avenue
Chicago, Illinois 60601-6731
(312) 616-5600 (telephone)
(312) 616-5700 (facsimile)

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